REMARKS/ARGUMENTS

1.) Claim Status

Claims 1, 2, 4-12, 14-18, and 20-23 are pending in the application. The claims have not been amended. Favorable reconsideration of the application is respectfully requested in view of the following remarks.

2.) Claim Rejections – 35 U.S.C. § 103(a)

On Page 2 of the Office Action, the Examiner rejected claims 1-2, 4-5, 7-12, 14, 17-18, 20-21, and 23 under 35 U.S.C. § 103(a) as being unpatentable over Chatterjee et al. (US 5,634,046) in view of Jacobson, et al. (US 7,206,925). The Applicants appreciate the Examiner's thorough Office Action, but respectfully disagree that the combination of Chatterjee and Jacobson teaches or suggests the claimed invention.

In the Applicant's previous response, it was argued that the cited references did not disclose a dedicated direct path between the special-purpose register file and the memory for loading the special-purpose register file from memory. The Examiner has cited a new reference, Jacobson, and contends this feature is shown by Jacobson (FIG. 3, backing register file 300 and connection 304 to main memory 306).

However, FIG. 3 shows connection 304 to be a 1-way connection from the backing register file to the main memory. In addition, Jacobson teaches in column 5, lines 17-23 that the purpose of this configuration is that the backing register file 300 can be used to release execution units and their associated register files 308 or 310 as soon as values are written out of the register files 308 or 310 to the backing register file 300, and then letting the values in the backing register file be written to main memory using the needed additional clock cycles.

The Applicant's claims recite that the dedicated direct connection between the special-purpose register file and the memory is for loading the special-purpose register file with memory address calculation information ***from*** memory. The purpose is to speed up memory accesses rather than Jacobson's purpose of accelerating the release of execution units and their associated register files. Thus, the recited connection is

operating in the opposite direction, for an entirely different purpose, and achieves a different result than the Chatterjee/Jacobson combination. Thus, there is still no disclosure or suggestion in the prior art of a dedicated direct path between said special-purpose register file and memory *for loading the special-purpose access register file from memory.*

This limitation is recited in each of the Applicant's independent claims as follows:

Claim 1: "wherein said at least one dedicated interface includes a dedicated direct path between said special-purpose register file and memory for loading said special-purpose access register file from memory;"

Claim 15: "wherein said first dedicated interface includes a dedicated direct path between said special-purpose register file and the dedicated cache for loading said special-purpose access register file from the dedicated cache;"

Claim 17: "transferring memory address calculation information in relation to said special-purpose register file via at least one dedicated interface associated with said special purpose register file, wherein said at least one dedicated interface includes a dedicated direct path between said special-purpose register file and memory for loading said special-purpose access register file from memory;".

Therefore, the withdrawal of the § 103 rejection and the allowance of independent claims 1, 15, and 17 are respectfully requested.

Claims 2, 4-5, 7-12, 14, 18, 20, 21, and 23 depend from base claims 1 and 17 and recite further limitations in combination with the novel and unobvious elements of claims 1 and 17. Therefore, the allowance of claims 2, 4-5, 7-12, 14, 18, 20, 21, and 23 is respectfully requested.

On Page 22 of the Office Action, the Examiner rejected claims 6, 15-16, and 22 under 35 U.S.C. § 103(a) as being unpatentable over Chatterjee in view of Jacobson and further in view of Aikawa et al. (US 5,371,865). The Examiner cited Aikawa for disclosing an intermediate or cache memory. However, like Chatterjee and Jacobson, Aikawa also fails to disclose or suggest a dedicated direct path between said special-purpose register file and memory *for loading the special-purpose access register file*

from memory. Thus, the Chatterjee/Jacobson/Aikawa also fails to establish a *prima facie* case of obviousness as required by MPEP 2143.

As noted above, this limitation is recited in independent claims 1, 15, and 17. Therefore, the withdrawal of the § 103 rejection and the allowance of independent claims 1, 15, and 17 are respectfully requested.

Claims 6, 16, and 22 depend from base claims 1, 15, and 17, respectively, and recite further limitations in combination with the novel and unobvious elements of claims 1, 15, and 17. Therefore, the allowance of claims 6, 16, and 22 is respectfully requested.

3.) Prior Art Not Relied Upon

On Page 32 of the Office Action, the Examiner stated that the prior art made of record and not relied upon is considered pertinent to the Applicants' disclosure. However, the Applicant's reading of these references has not revealed any teaching or suggestion of a computer system having a dedicated direct path between said special-purpose register file and memory for loading the special-purpose access register file from memory.

4.) Conclusion

In view of the foregoing remarks, the Applicants believe all of the claims currently pending in the Application to be in condition for allowance. The Applicants, therefore, respectfully request that the Examiner withdraw all rejections and issue a Notice of Allowance for claims 1, 2, 4-12, 14-18, and 20-23.

The Applicants request a telephonic interview if the Examiner has any questions or requires any additional information that would expedite the prosecution of the Application.

Respectfully submitted,

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